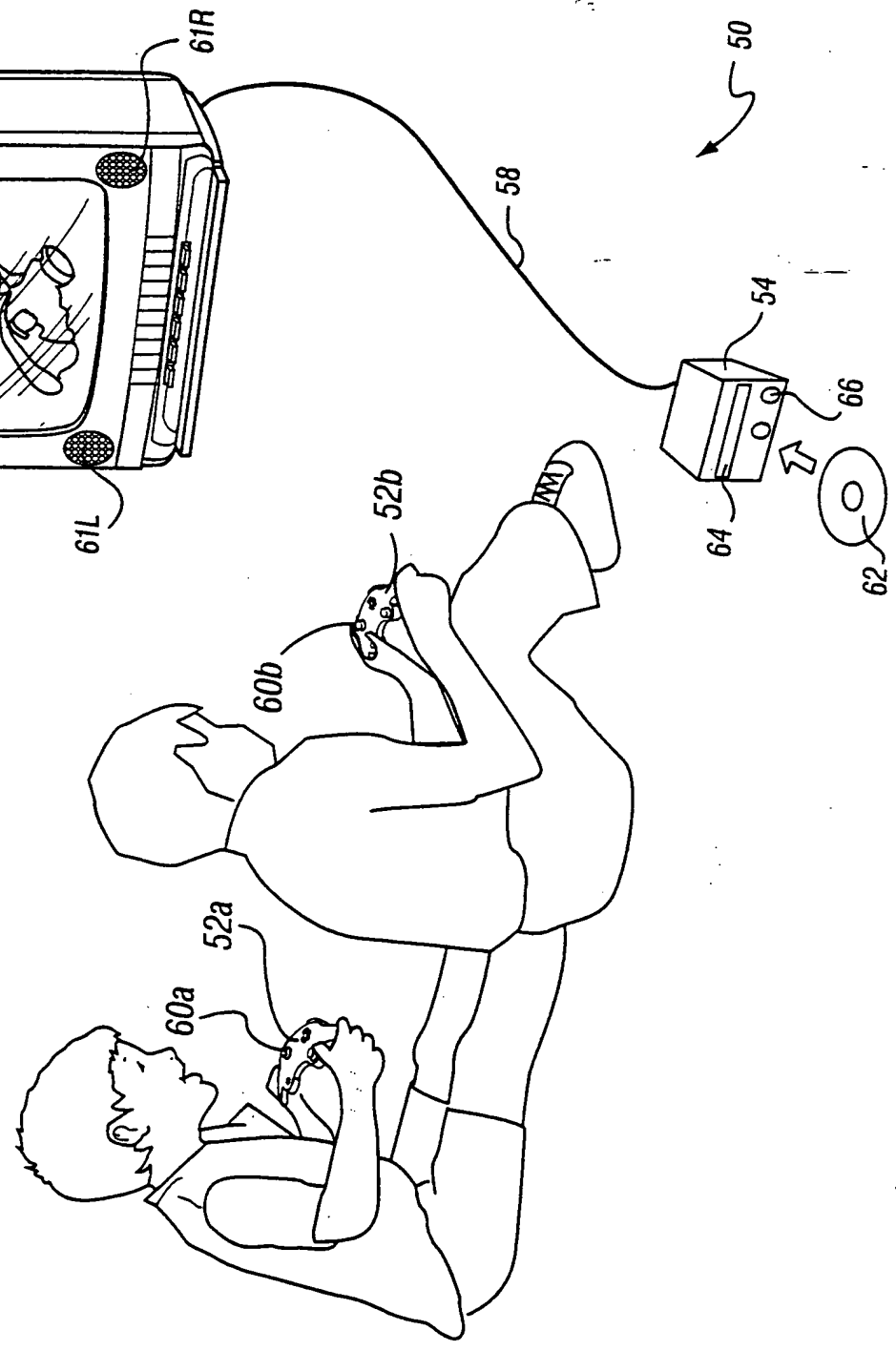


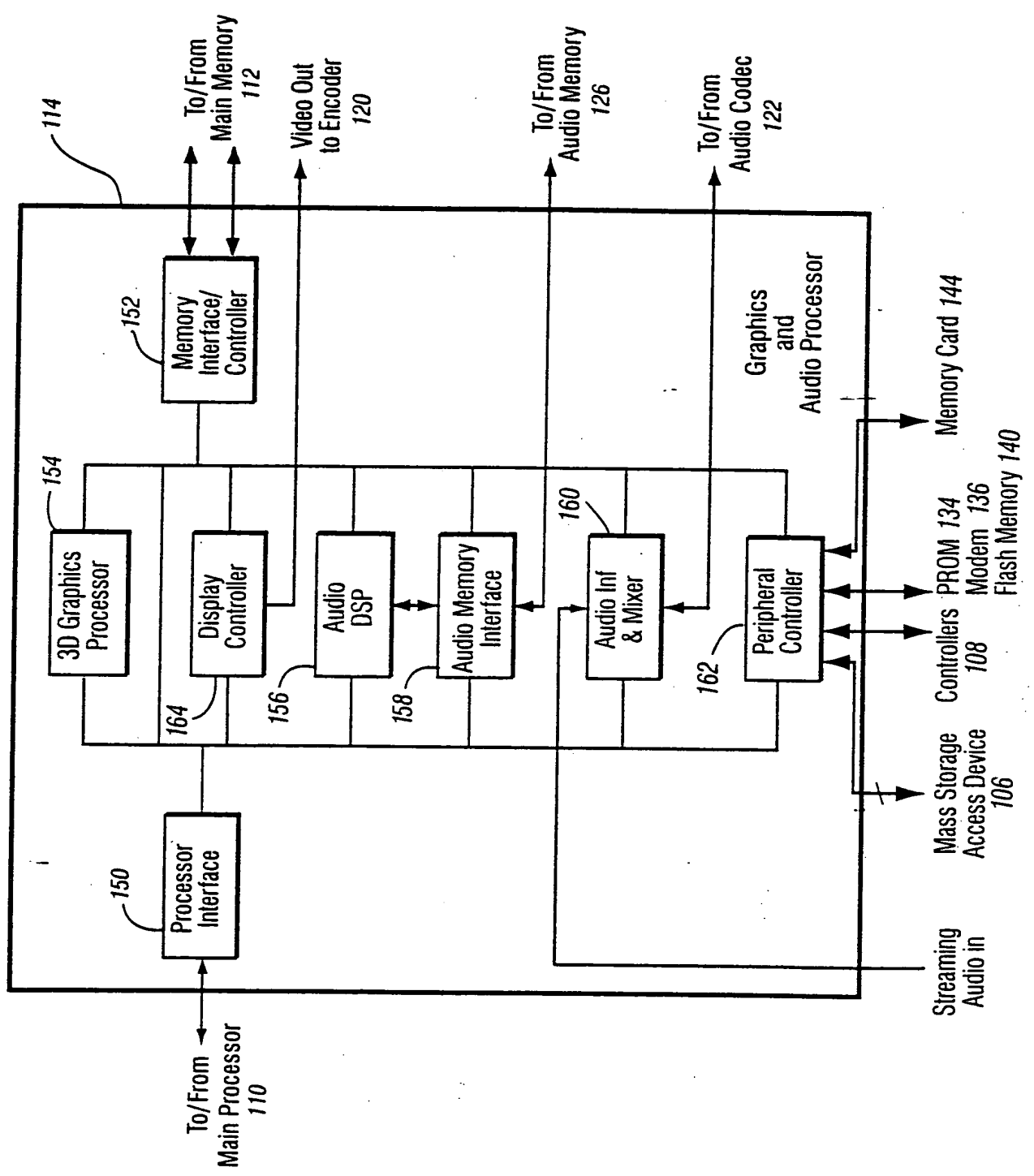
FIG. 1

Fig. 1



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Fig. 3



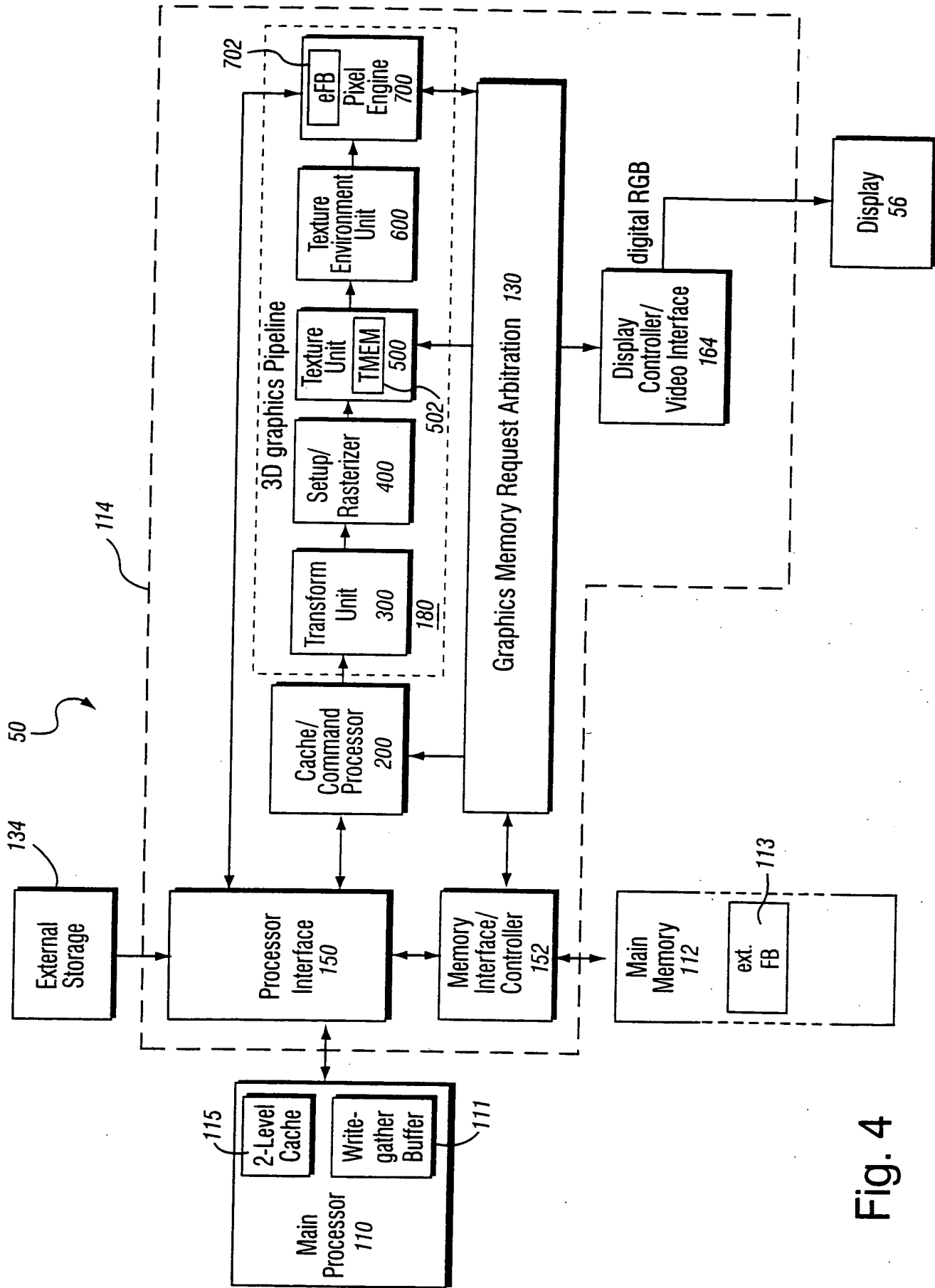


Fig. 4

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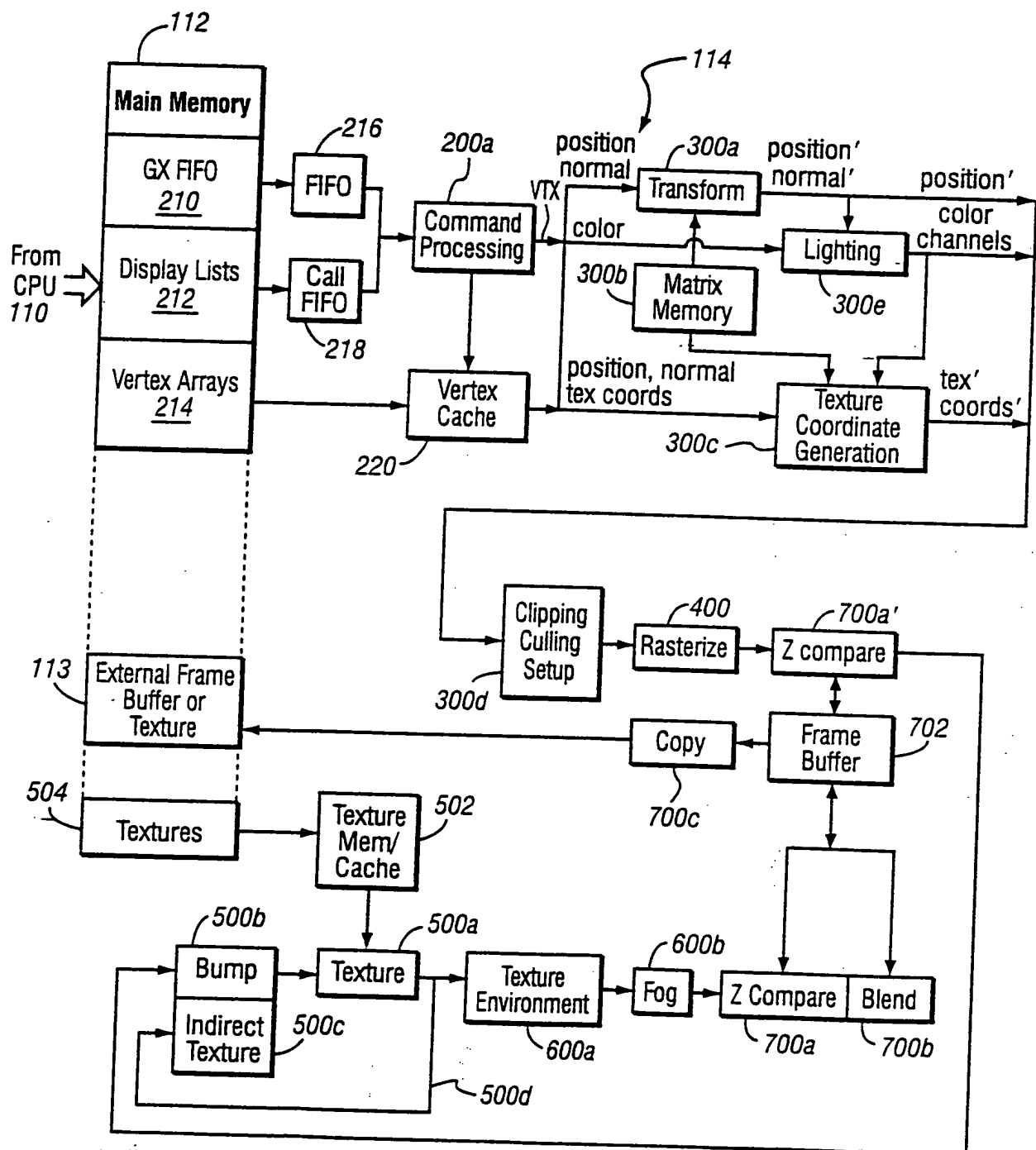
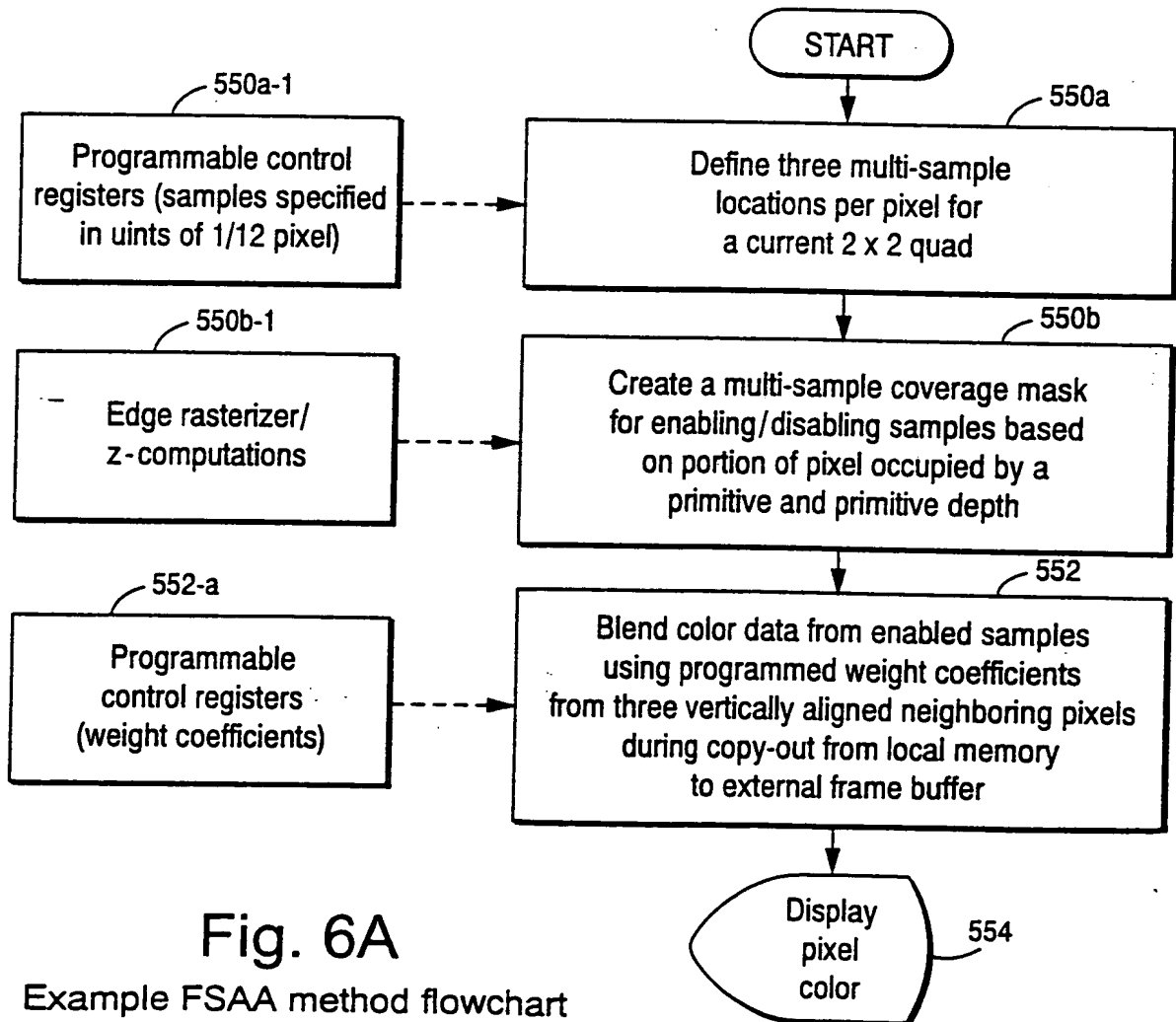
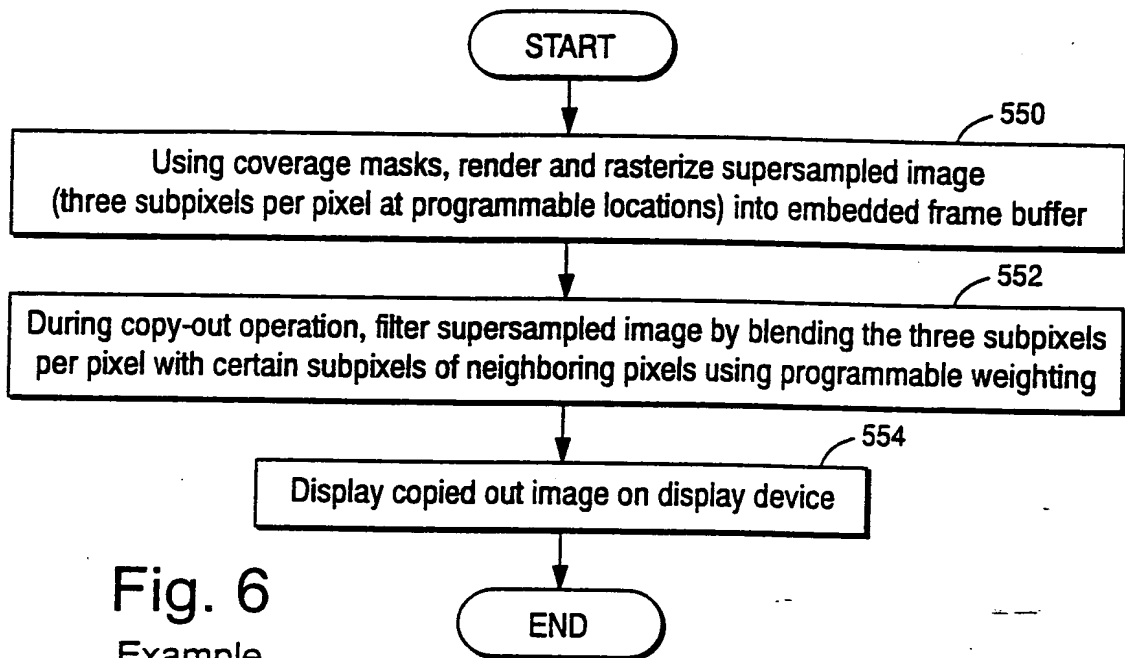


Fig. 5 EXAMPLE GRAPHICS PROCESSOR FLOW

[illegible]

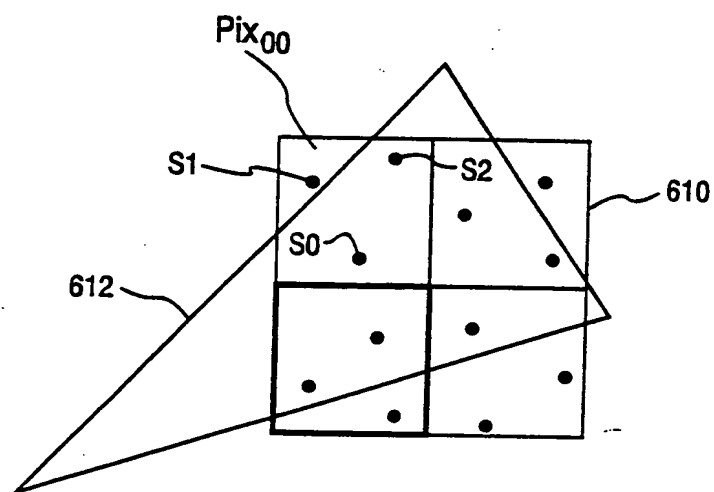
[illegible]

Fig. 7
(Primitive and super-sampled pixel quad)

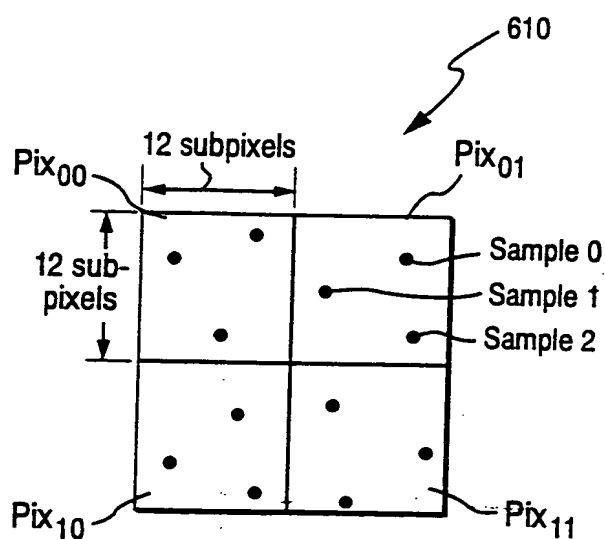


Fig. 8
(Sampling pattern)

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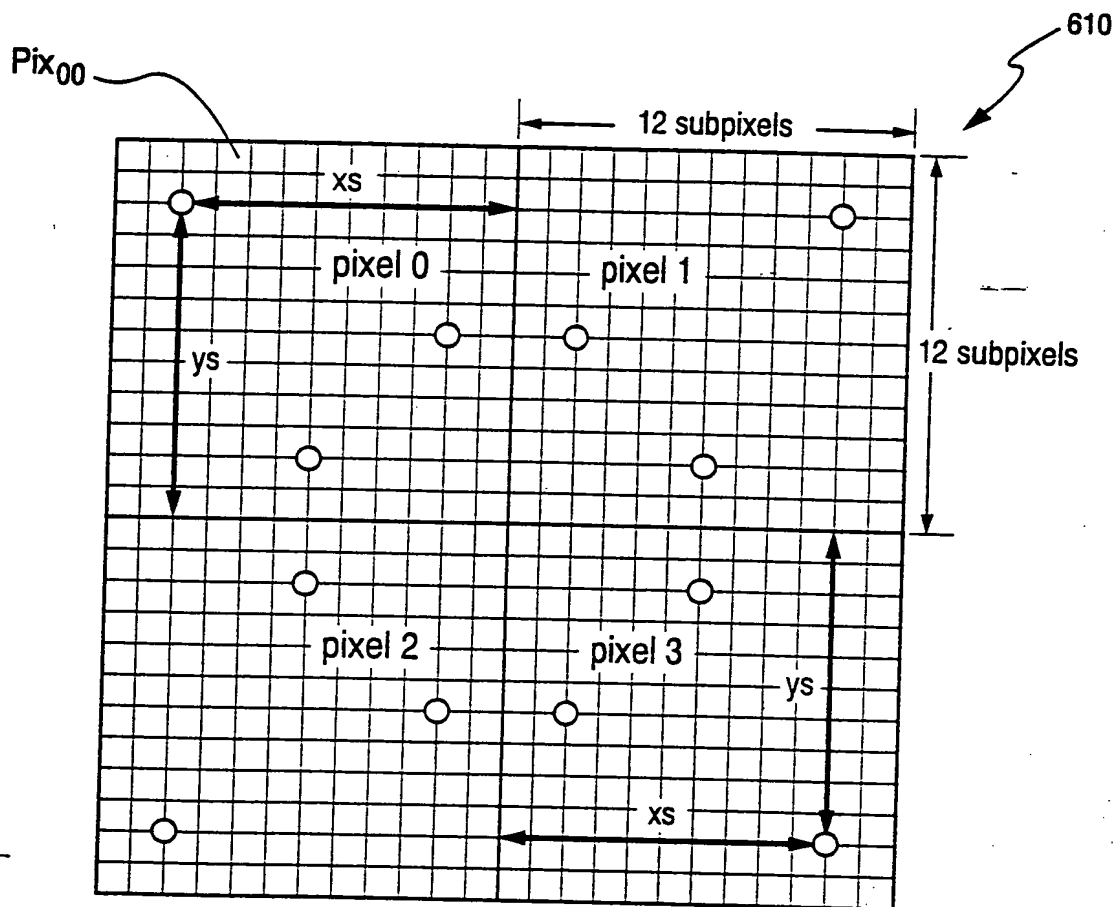


Fig. 9 (Super-sample locations in units of 1/12 pixel)

[illegible]

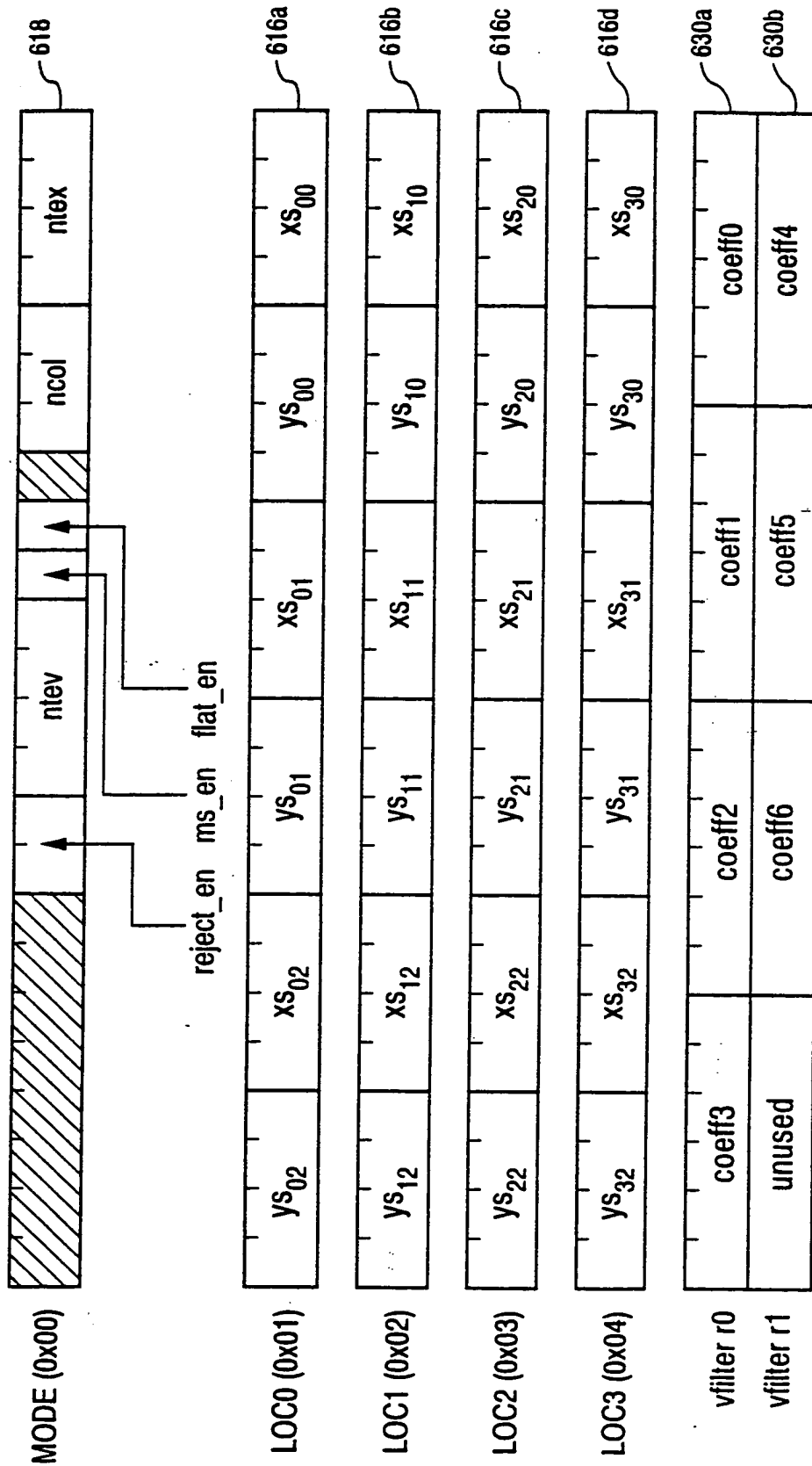
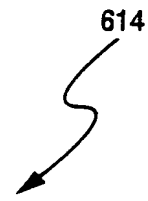


Fig. 11 (Programmable control registers for setting sample locations & filter coefficients)

[illegible]

The diagram illustrates a copy pipeline for video processing. It consists of several components connected in a sequence:

- 702 EFB (Embedded frame buffer)**: The starting point of the pipeline.
- 620**: A label with an arrow pointing to the first processing block.
- 622 antialias deflicker**: The first processing block, which contains a sub-component labeled **628 filter state**.
- 624 RGB to YUV**: The second processing block.
- 626 Y scale**: The third processing block, which contains a sub-component labeled **scale**.
- 113 XFB (External frame buffer)**: The final destination of the pipeline.

A large arrow at the bottom, labeled **copy pipeline**, indicates the direction of data flow from left to right through the processing blocks.

Fig. 13 (Copy-out pipeline)

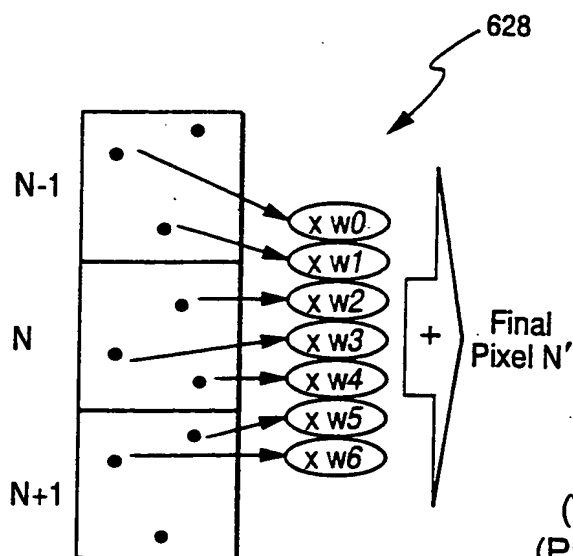


Fig. 14
(Vertical Filter Blending)
(Programmable 7-tap filter)

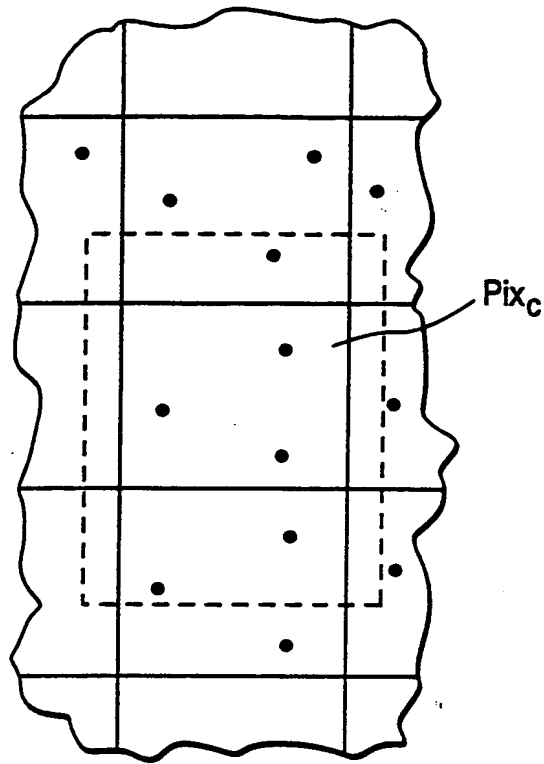


Fig. 15
Example vertical filter aperture

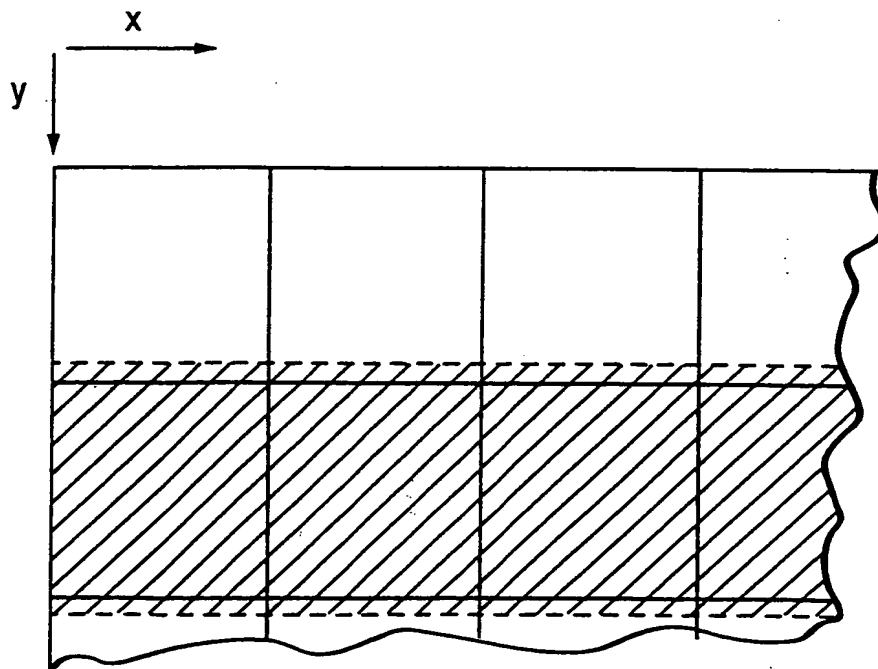
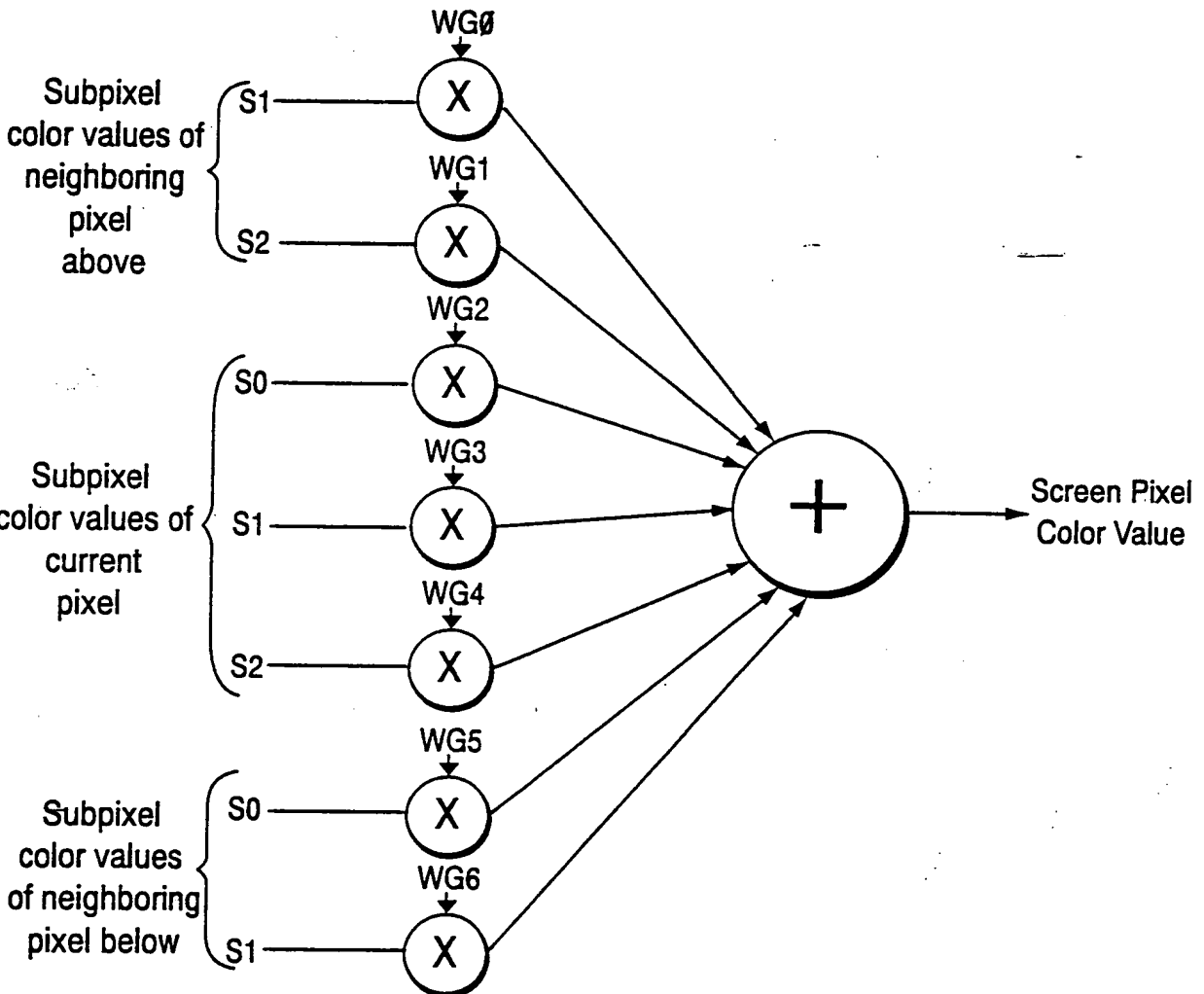


Fig. 17
Example AA copy out buffering

Fig. 16



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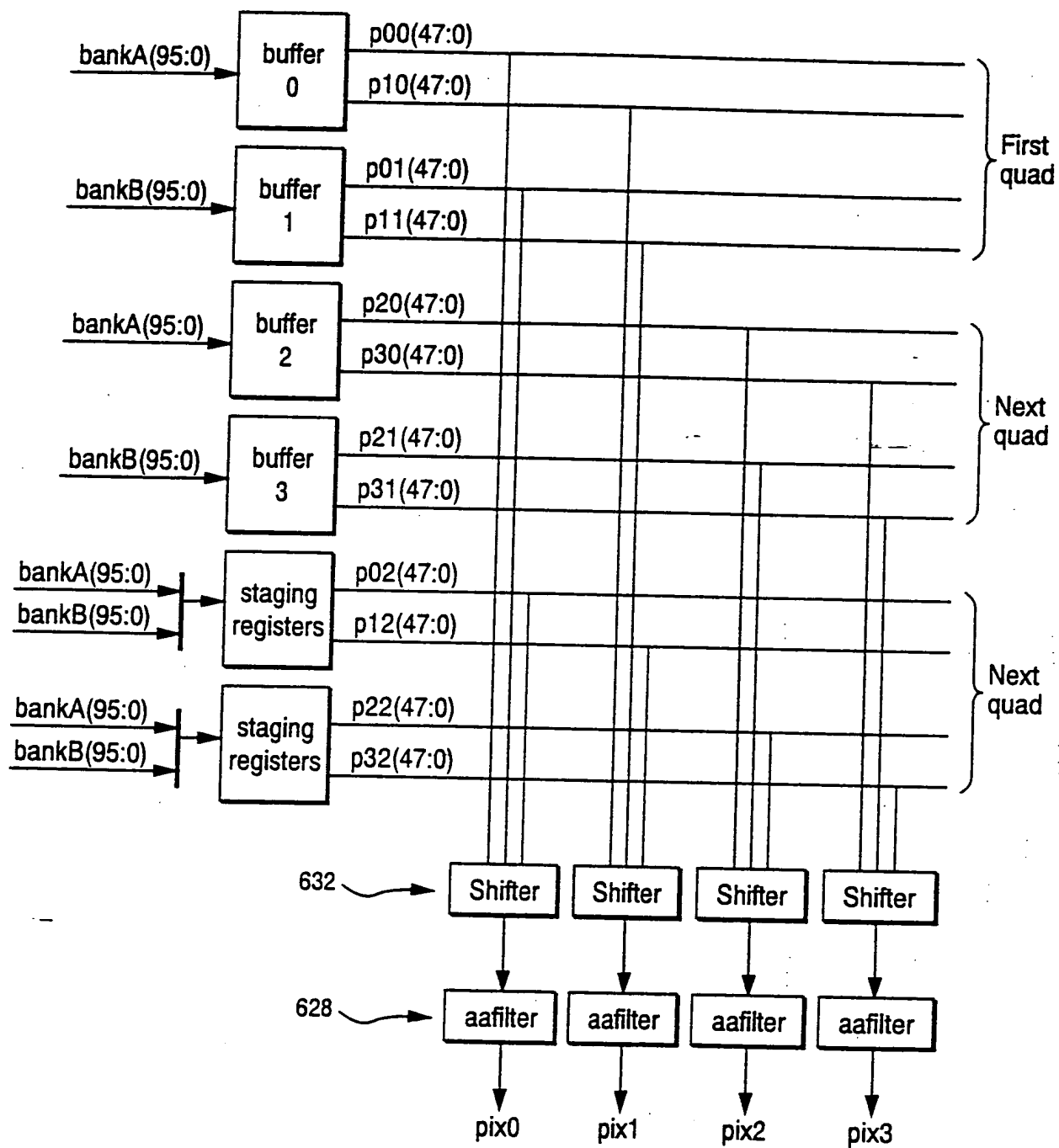


Fig. 18
(AA buffering)

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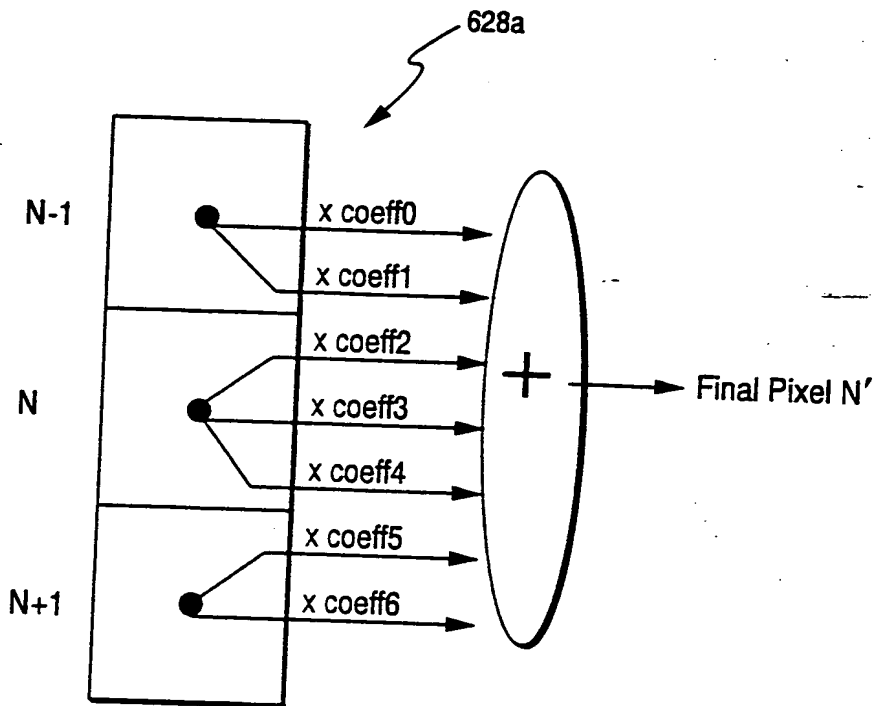


Fig. 19
Example de-flickering filter

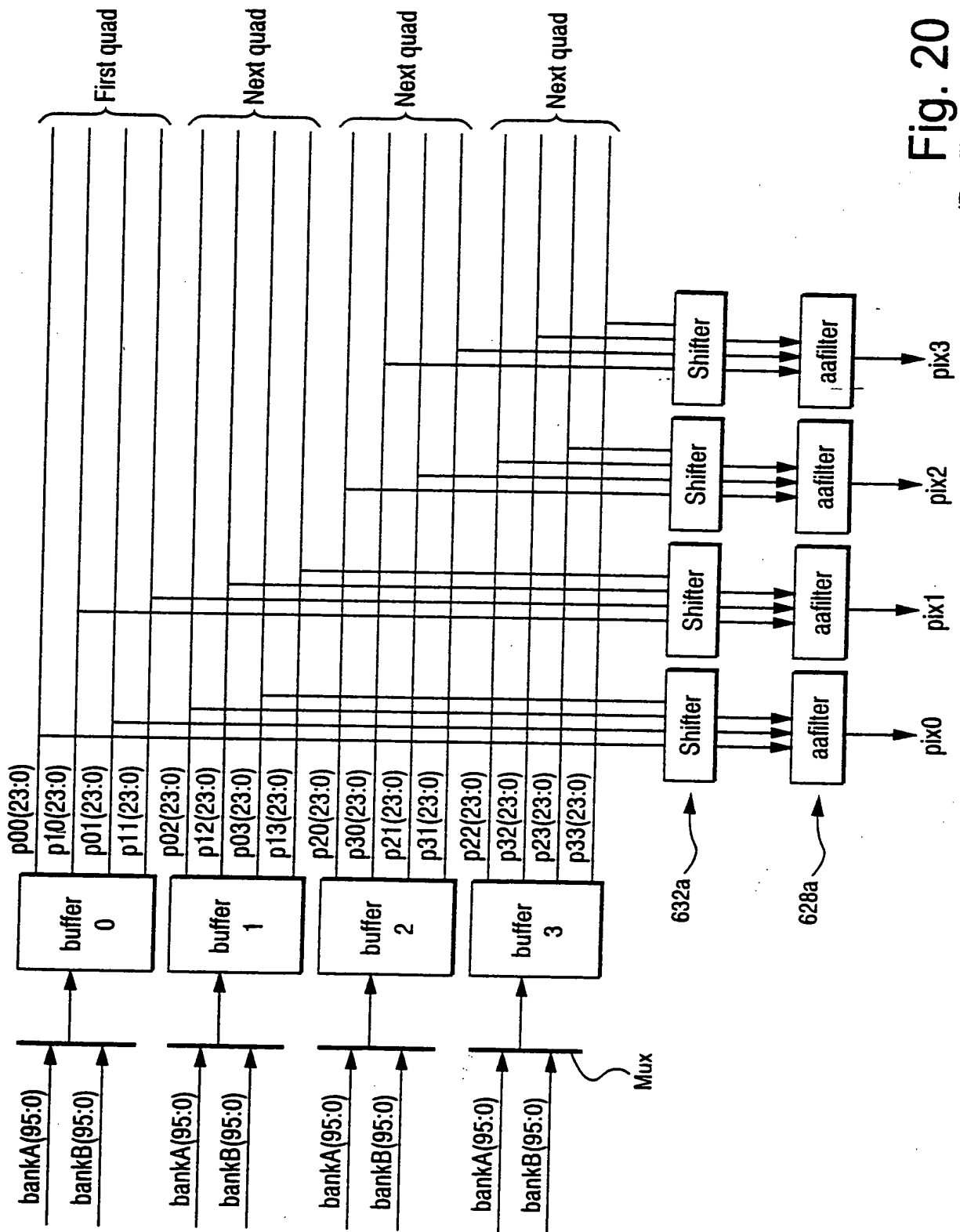


Fig. 20
(De-flicker buffering)

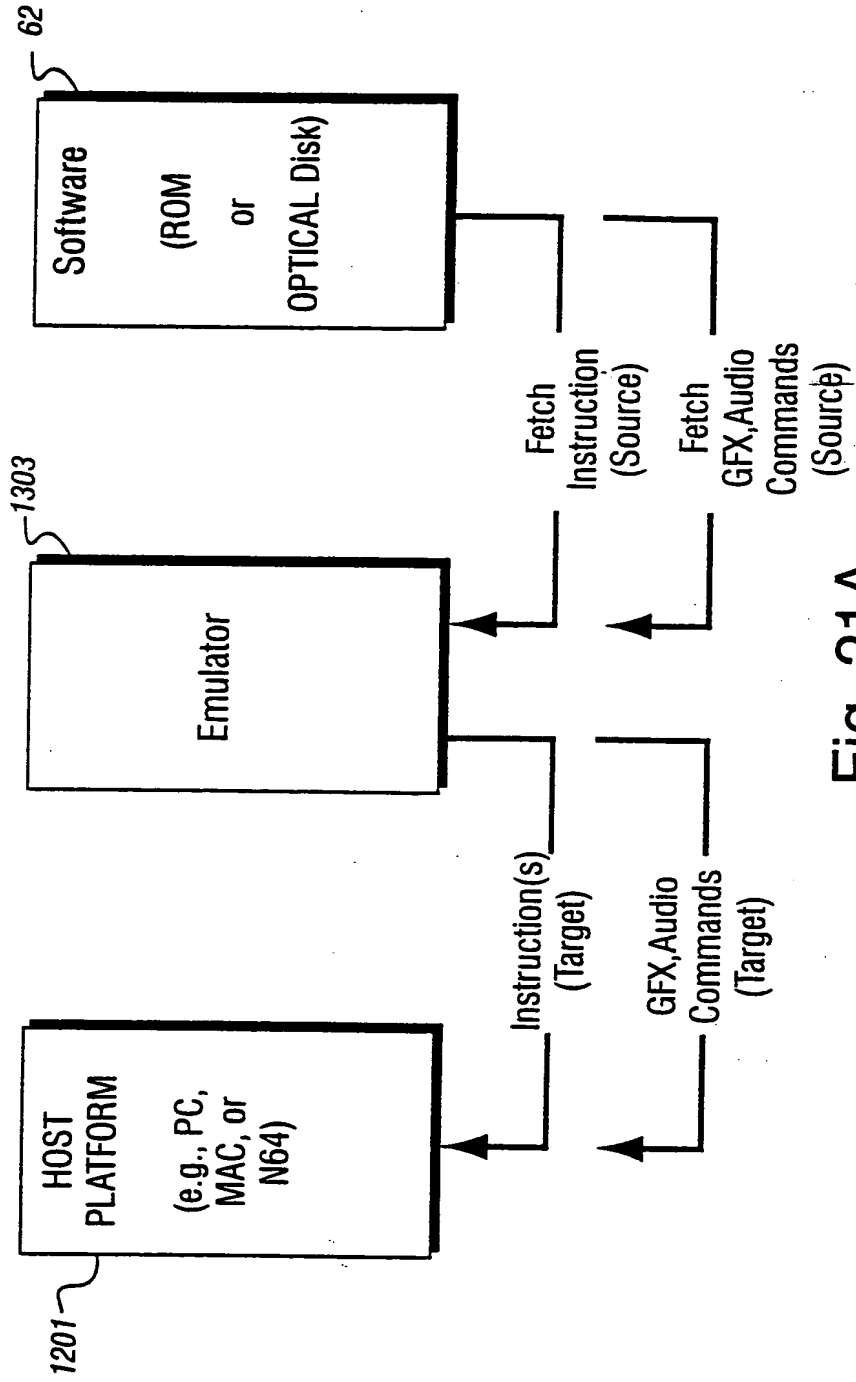


Fig. 21A

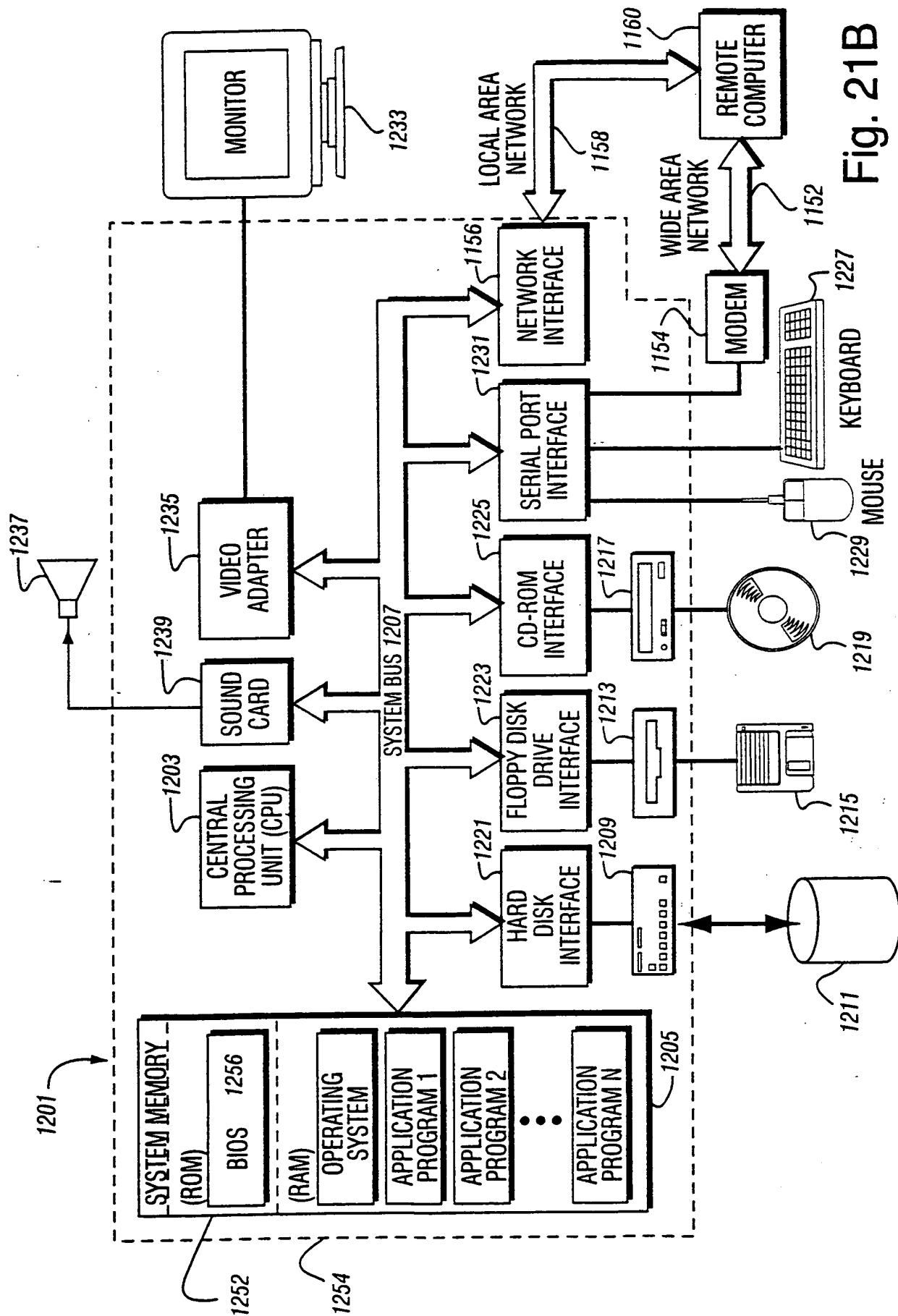


Fig. 21B